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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QIN, YIXING	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,043	BLUMER, MARC	
	Examiner	Art Unit	
	Yixing Qin	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-13, and 19-22* is/are rejected.

7)☒ Claim(s) *3-7 and 14-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02 December 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Allowable Subject Matter

Claims 3-7 and 14-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Objections

Claim 21 is objected to because of the following informalities: Claim 21 should end with a period. Appropriate correction is required.

Claim 22 is objected to because of the following informalities: the claim should read "The system of Claim 12..." not "Claim 1" as currently written. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

I. Claims 1, 2, 8-13, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's disclosed prior art in the background and in view of Yano (U.S. Patent No. 5,798,720).

The Yano reference discloses a converter circuit that can effectively reduce the frequency of a clock pulse to one half while maintaining the same data rate and operation speed. One would understand that keeping the frequency of the clock pulse "normal" would double the data rate and operation speed.

1. **Claim 1**

A method of increasing resolution of an image-forming device, comprising the steps of:

- **applying a signal representing at least a portion of a source image to a data selecting means, so that each bit of the signal corresponds to an input to the data selecting means;**
- The applicant discloses in the prior art of the background on page 2, lines 6-10 of the applicant's specification that pulse width modulators (PWMs) are commonly used in laser printers and that "[d]igital data specifying grayscale values of the pixels to be printed is supplied to the pulse width modulator, and the pulse width modulator outputs a signal that varies the width, and also the period of the laser pulses, producing variably sized and spaced dots." The applicant does not further disclose the design of PWMs in the prior art section.
- However, the Yano reference discloses in Fig. 2A a diagram showing that a parallel data input 11 inputs data into an F/F 13 (input circuit made from n flip-flops – column 4, lines 48-51). Fig. 2A further shows that the data is then

inputted into an n-to-1 multiplexer. Although this circuit is not explicitly called a PWM, it serves the purpose of one in that it an incoming signal into a different output signal. One skilled in the art would know that one can substitute similar parts in an electronic device (i.e. place this circuit in the Yano reference in place of a PWM in a printer).

- Yano also discloses in column 3, lines 63-66 that "...the parallel data input terminal is provided for n bits." This data could be image data since image data is made up of bits and is well-known in the art. Furthermore, image data would be the type of data being processed in a laser printer. One would understand that the input circuit 13 takes n bit inputs and produces n bit outputs to the n-to-1 multiplexer.
- **at each of a rising and falling edge of a clock pulse, selecting a data input, wherein each of the inputs is selected;**
- The applicant discloses that digital PWMs typically operate on the rising clock edge only (page 3, lines 9-10 of the applicant's specification). However, the applicant does not disclose anything in the prior art relating to the operation of a PWM on both the rising and the falling edge of the clock.
- However, the secondary reference, Yano, discloses in column 3, lines 66-67 and column 4, lines 1-6 that "...circuit 17 which produces, from a basic clock pulse signal having a frequency of f/2 Hz, a byte clock pulse signal Byte Clock0 having the same phase as that of the basic clock pulse signal and another byte clock

pulse signal Byte Clock1 having an opposite phase inverted from that of the basic clock pulse signal." One can see circuit 17 in Fig. 2A.

- Furthermore, in column 4, lines 44-48 that "...a logical OR circuit 19 which receives outputs 1 and 2 of the rising edge detection circuits 18a and 18b and whose output 3 serves as a byte clock pulse signal of a frequency f Hz." Basically, the rising edges of Clock0 (same pulse) and Clock1 (inverted pulse) is the same as the rising and falling edges of the basic input clock (Fig. 2A)
- Furthermore, in column 5, lines 18-20, Yano discloses that "[t]he byte clock pulse signal (3) is applied as a driving pulse signal to the input circuit 13..." One would understand that the data coming in (item 11 in Fig. 2A) would be transferred to circuit 13 (i.e. **"data is selected"**).
- **inputting the data bit corresponding to the selected data input to the data selecting means;**
- Again, the applicant's prior art in the background does not explicitly disclose how a PWM circuit works.
- Yano discloses in column 5, lines 21-23 that "...the parallel data inputted from the parallel data input terminal 11 are fetched by the input circuit 13 and then inputted to the multiplexer 14."
- **and transmitting the data bit to a light-emitting element, so that 2 bits are output to the light-emitting element for each clock cycle;**

- As mentioned before in limitation 1, the applicant disclosed that the signal from a PWM varies the width and period of a laser. However, the applicant does not disclose that 2 bits are outputted per cycle.
- Yano discloses that the frequency of the basic clock is f/2 (column 4, lines 1-2) and the rate that the input data comes in is f (column 3, line 66). Furthermore, in column 4 lines 58-61 that "[t]he PLL synthesizer 15 receives the byte clock pulse signal (3) and generates a bit clock pulse signal having a frequency of n*f Hz equal to n (n is the number of bits in the input data – column 3, line 64) times that of the byte clock pulse signal (3)."
- One can see from Fig. 2A that he output from the PLL is the selector for the n-to-1 MUX (item 14). In column 5, lines 29-31 that "...the n-bit parallel data are outputted serially one after another one bit from the multiplexer 14. The data rate is then n*f bps..." One would understand that the output data rate is at least f (if n is one bit), which is twice as fast as the clock speed (i.e. a clock rate of f/2 can process data coming in at rate f, which means the multiplexer would output 2 bits per clock cycle).
- **wherein the output specifies any width of and interval between light pulses emitted by said light-emitting element.**
- As mentioned before in limitation 1, the applicant disclosed that the signal from a PWM varies the width and period of a laser.
- Since both reference are in the art of performance enhancement of data modulation, it would have been obvious to one of ordinary skill in the art at the

time of the invention to use a PWM with a design such as the one in the Yano reference in place of an existing PWM design in a laser printer. This reason would serve as the motivation for the combining of the two references for the claim rejections to follow this one.

- The motivation would be to use a faster design in place of an older design (i.e. similar to upgrading a computer with a faster CPU).

2. Claims 2 and 13

The method (system) of claim 2 (12), wherein

- **the data-selecting means comprises a multiplexer having sixteen data inputs, and wherein said data signal comprises sixteen bits.**
- Although the applicant discloses the workings of PWMs, he does not disclose how one is made up.
- As mentioned above in the rejection to claim 1, Yano disclosed that data of n-bits can be processed by an n-to-1 multiplexer, and n could be any reasonable number of bits (i.e. 16) Thus, one skilled in the art at the time of the invention could have chosen 16-bits (or any reasonable number) for the input of the PWM. The motivation would be to use the signal outputted to more accurately define the width and period of a laser.

8. Claims 8 and 19

The method (system) of claim 1(12), wherein

- **the image-forming device comprises a laser printer and wherein the light-emitting device comprises a laser.**
- Again, from the rejection to claim 1 above, the applicant as disclosed in the background that PWMs are well known to control lasers in laser printers.

9. Claims 9 and 20

The method (system) of claim 1 (12), wherein

- **the portion of the source image comprises a pixel, and wherein a pixel is specified by a 16-bit value.**
- Although the applicant discloses that the pixel data loaded into a PWM have only 8-bits (page 3, lines 6-9 of the applicant's specification), it does not disclose that the current PWMs could handle a 16-bit pixel data input.
- As mentioned above in the rejection to claims 2 and 13, the circuit in Yano's reference can take any n-bit input. It would be a design choice to specify the value by 16-bits instead of 8-bits.
- The motivation would be that 16-bits better define values than 8-bits (i.e. more accurately determines pulse width/periods for a laser)

10. Claims 10 and 21

The method (system) of claim 1(12), said method (system)

- **implemented in a circuit comprising discrete components (comprising a circuit composed of discrete components)**

- Again, the applicant does not disclose in the prior art of the background the make-up of the PWM circuit. However, one can see from Fig. 2A of the Yano reference that there are discrete components in the circuit.
- The motivation to use discrete components would allow different combinations of components for varying operational functions (such as varying functioning speed) and to ease repair on circuitry (i.e. need only to replace one broken component, not replace entire PWM).

12. Claim 12

A system for increasing resolution of an image-forming device, comprising:

- **data selecting means having a plurality of inputs and at least one output, each input corresponding to one bit of a signal applied to the data selecting means, the signal representing at least a portion of a source image;**
- From the rejection to claim 1 above, the examiner has made the case of obviousness of using the Yano circuit as a PWM in a laser printer. One skilled in the art would understand that data used in printers would likely be image data.
- Also, in Fig. 2A of Yano, item 13 is made of n flip-fops (column 5, line 20) and item 14 is an n-to-1 MUX. Column 5, lines 21-23 that "...the parallel data inputted from the parallel data input terminal 11 are fetched by the input circuit 13 and then inputted to the multiplexer 14." One would understand that the MUX has n one-bit inputs and each would correspond to one bit of an inputted signal.

- **a clock signal;**
- Yano discloses in Fig. 2A a basic clock pulse.
- **and means for selecting a data input at each of a rising and falling edge of the clock signal, wherein each of the inputs is selected and the corresponding bit input to the data selecting means so that 2 bits are output to a light-emitting element of the image-forming device for each clock cycle, the output specifying any of width of and intervals between pulses emitted by said light-emitting element.**
- This limitation is essentially a combination of the second, third and fourth limitations of claim 1. Please refer to the rejection to those limitations in claim 1.
- The motivation would be to use a faster design in place of an older design (i.e. similar to upgrading a computer with a faster CPU).

II. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's disclosed prior art in the background and in view of Yano (U.S. Patent No. 5,798,720) and further in view of Official Notice.

11. Claims 11 and 22

The method (system) of claim 1 (12), said method (system)

- **implemented in (comprising) a programmable logic device (PLD).**
- Although neither the applicant nor the Yano references explicitly discloses the use of PLDs to create an PWM. The examiner takes official notice that PLDs are

essentially premade, programmable circuits that are created from arrays of gates and the use of PLDs such as PROMs and FPGAs are old and well-known.

- The motivation for using PLDs would be that using premade circuits could be less costly than designing and building an entirely new circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yixing Qin whose telephone number is 703-306-4142. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Coles can be reached on 703-305-4712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YQ

JOSEPH MANCUSO
PRIMARY EXAMINER